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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,384	03/26/2004	Sung-Fei Wang	WANG3232/EM	7610

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/809,384	WANG, SUNG-FEI	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *5 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-16, 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-4, 10-12, 13, 15, 16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claim 18 have been fully considered but they are not found persuasive. Rejection of this claim has been made clearer in this action.

Applicant's arguments with respect to claims 6-9 and 14 have been fully considered but they are not persuasive. There is motivation to provide an intermediate area in a solder ball array in the prior art reference of Barrow, outlined in Col 2 Ln 59-66, which has been cited in this action. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 12, 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (U.S. Patent #6225702), in view of Yano et al (U.S. Patent #6046499).

With respect to **claims 1-4, 12, 13, 15, and 16**, Nakamura teaches a substrate having an upper surface and a lower surface (Fig. 3, 5), wherein the substrate has a first central area (Fig 4, 3a) and a first peripheral area encompassing the first central area (Fig. 4, 3b and 3c); a chip having an active surface (Fig. 3, 1), wherein the active surface has a second central area (Fig. 4, 3a) and a second peripheral area encompassing the second central area (Fig. 4, 3b and 3c); a plurality of electrically conductive bumps connecting the first peripheral area and the second peripheral area (Fig. 4, 3b and 3c);

that the first central area is rectangular (Fig. 4, 3a) as set forth in claim 2;

that the first peripheral area is ring-like (Fig. 4, 3b and 3c), as set forth in claim 3;

that the substrate further comprises a first intermediate area between the first central area and the first peripheral area, and the first intermediate area is ring like (Fig. 4, exposed area between 3a and 3b,c), as set forth in claim 4;

that the reinforced bumps comprise metal bumps (Col 3 Ln 44), as set forth in claim 12;

that the reinforced bumps comprise metal bumps (Col 3 Ln 44) and it is inherent that metal is thermally conducting, thus one reinforced bump is a thermally conductive bump, as set forth in claim 13

that the electrically conductive bump is a sphere (Col 2 Ln 17) and the first intermediate area has a width that is substantially equal to the double of a diameter of the electrically conductive bump (Fig. 5, width taken from innermost ball 3c to outermost ball 3a), as set forth in claim 15;

that the one of the inner bumps is a sphere (Col 2 Ln 17) and a distance between the innermost electrically conductive bump and the outermost reinforced bump is substantially equal to the double of a diameter of the reinforced bump (Fig. 5, width taken from innermost ball 3c to outermost ball 3a), as set forth in claim 16;

Nakamura does not teach a plurality of reinforced bumps interposed between the chip and the substrate with no electrically conductive function, wherein the reinforced bump connects the first central area and the second

central area. Yano teaches a configuration of solder ball electrodes wherein solder balls in a central area have no electrically conductive function (Fig. 5A, 29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the package of Nakamura with solder balls to connect the first and second central area, wherein the solder balls have no electrically conductive function as taught by Yano in order to improve the heat transfer characteristics of the package.

Claims 6-9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Yano, in view of Barrow (U.S. #5894410).

With respect to **claim 6**, Nakamura and Yano teach all of the limitations of claim 4, but do not teach that the first intermediate area has a width at least larger that the double of the width of the electrically conductive bump. Barrow teaches a solder bump configuration wherein the first intermediate area (Fig. 4, 42) has a width at least larger than the double of a width of the electrically conductive bump (Fig. 4, 34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the width of the first intermediate area of Nakamura as taught by Barrow to reduce mechanical stress on the electrically conductive bumps (Col 2 Ln 59-66).

With respect to **claim 7**, Nakamura and Yano teach all of the limitations of claim 1, but do not teach a distance between the innermost electrically

conductive bump and the outermost reinforced bump that is at least larger than the double of a width of the reinforced bump. Barrow teaches a distance between an inner bump and an outer bump to be larger than the double of a width of an inner bump (Fig. 4, 42)). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the distance between the innermost electrically conductive bump and the outermost reinforced bump of Nakamura as taught by Barrow to reduce mechanical stress on the electrically conductive bumps (Col 2 Ln 59-66).

With respect to **claim 8**, Nakamura and Yano teach all of the limitations of claim 4, furthermore Nakamura teaches spherical conductive bumps (Col 2 Ln 17). Nakamura and Yano do not teach a first intermediate area with a width at least larger than a diameter of a conductive bump. Barrow teaches a width as described above being at least larger that a diameter of a conductive bump (Fig. 4, 42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the width of the first intermediate area of Nakamura as taught by Barrow to reduce mechanical stress on the electrically conductive bumps (Col 2 Ln 59-66).

With respect to **claim 9**, Nakamura and Yano teach all of the limitations of claim 1, and furthermore Nakamura teaches spherical conductive bumps (Col 2 Ln 17). Nakamura and Yano do not teach a distance between the innermost electrically conductive bump and the outermost reinforced bump that is at least larger than the double of a diameter of the reinforced bump. Barrow teaches a

distance as described above being at least larger than the double of a diameter of a reinforced bump (Fig. 4, 42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the distance between the innermost electrically conductive bump and the outermost reinforced bump of Nakamura as taught by Barrow to reduce mechanical stress on the electrically conductive bumps (Col 2 Ln 59-66).

With respect to **claim 14**, Nakamura and Yano teach all of the limitations of claim 1, but do not teach a solder ball formed on the lower surface of the substance. Barrow teaches a solder ball formed on the lower surface of the substrate (Col 1 Ln 57-59). It would have been obvious to one of ordinary skill in the art at the time the invention as made to place solder balls on the lower surface of the substrate in order to facilitate connection to a printed circuit board.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura and Yano, in view of Caletka et al (U.S. #6104093), hereafter known as Caletka.

With respect to **claim 10**, Nakamura and Yano teach all of the limitations of claim 1, but do not teach an underfill disposed between the chip and the substrate and covering the electrically conductive bumps. Caletka teaches an underfill as described above (Col 4 Ln 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make a flip chip comprising an underfill disposed between the chip and the substrate and

covering the electrically conductive bumps as taught by Caletka in order to keep moisture from the conductive bumps and to reinforce the bumps.

With respect to **claim 11**, Nakamura and Yano teach all of the limitations of claim 1, but do not teach an underfill disposed between the chip and the substrate and covering the reinforced bumps. Caletka teaches an underfill as described above (Col 4 Ln 20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make a flip chip comprising an underfill disposed between the chip and the substrate and covering the reinforced bumps as taught by Caletka in order to keep moisture from the conductive bumps and to reinforce the bumps.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura, in view of Farnworth et al (U.S. #6558979), hereafter known as Farnworth.

With respect to **claim 18**, Nakamura teaches all of the limitations of claim 1, but does not teach reinforced bumps made of epoxy. Farnworth teaches bumps made of epoxy (Col 4 Ln 1-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make reinforced bumps out of epoxy (Col 2 Ln 11) in order to reduce the damaging effects of TCE mismatch.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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